

# DC/DC Converter

## Project Design Report

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## Abstract

The need for a DC/DC converter of this caliber is a great one. The future is looking towards alternative power sources all of which will need to be regulated in one form or another. To make this possible, a highly efficient low cost product will have to be designed. Among all the different converter designs only a few are capable of providing high power with high efficiency. The accepted design will provide this output with the least amount of total losses. This will be tested experimentally, first by computer simulation, and then in the laboratory with the application of non-linear loading. With the loading conditions a 400V output voltage (with a differential of 10V) and a 5kW power output must be held steady to achieve an acceptable end product. This will be difficult due to the 21-48V varying input voltage. An estimation of both labor and material costs has been made; this will be appended as the design process proceeds. At this stage only a rough estimate can be offered. If the product meets all of the set requirements, the project will be considered a complete success.

The following are the features of the DC/DC converter.

- 21-42V varying input voltage, to simulate a real fuel cell
- Semiconductor switching
- Highly efficient transformer
- Full Bridge rectifier
- 400V, 5kW fully regulated output
- Fully self sufficient system

## Introduction

### **Statement of Need:**

The Future Energy Challenge (FEC) team of The University of Akron will be competing in the spring of 2005 with a Fuel Cell Inverter. The Fuel Cell Inverter is an alternative energy source. In developing countries where power utilities may not be readily available, the Fuel Cell Inverter may be the solution. Additionally, the Fuel Cell Inverter can act as a secondary power supply in events of power failure.

### **Problem Definition:**

**Goals:** The Fuel Cell Inverter is comprised of various components, one of which is a 10kW DC/DC converter. The team requires a constant 400V DC 5kW output with a varying 21-48V DC input to supply power to a varying load. For time and financial constraints the design team will design and build only one 5kW DC/DC converter. The design will allow two 5kW DC/DC converters connected in parallel to satisfy the 10kW specifications. The competing team, using the DC/DC team's design, may build the other 5kW DC/DC converter to satisfy the FEC's need for 10kW of power

**Objectives:** The design team will design and implement a DC/DC converter with a regulated output voltage. Our objectives are to design a converter with the following requirements:

- Cost efficient DC/DC converter
- Remain within the allocated budget
- Design product with minimum Mean Time To Failure rate of approximately 10 years
- 5kW power output
- 400V DC output with varying 21-48V DC input
- Output voltage tolerance within  $\pm 10V$

**Constraints:** The defined input voltage will vary between 21-48V DC and the permissible output voltage will be  $\pm 2.5$  percent of the stated regulated voltage of 400V DC. The DC/DC converter will be required to provide 5kW of power with a DC output voltage between 390-410V.

## **Design Requirements**

### **Requirement Specifications:**

The DC/DC converter will convert a varying input voltage to a fixed output. The input will consist of several lead-acid batteries connected in various configurations to produce the required input current. A high frequency transformer will be used to minimize the power loss. The DC/DC converter will be required to produce 5kW nominal power with at least 90% efficiency.

The control circuit of the DC/DC converter will measure the input and the output voltages as well as at the intermediate stages. If any fluctuations from the desired output voltage are present, the controller will vary the duty cycle to regulate the output voltage.

Due to the high frequency and high power involved in this design, cooling systems will be a requirement. The design shall have at least a Mean Time To Failure rate of approximately 10 years.

### **Summary:**

- 5kW nominal power output with 90% efficiency
- 400V DC output with a varying 21-48V DC input
- Output ripple voltage less than 1 percent
- High frequency transformer to minimize power loss
- Control circuit to maintain consistent output
- Cooling solutions: Heat sinks and Cooling Fans
- Circuit protection devices to limit current
- Output voltage tolerance within  $\pm 10V$
- Mean Time To Failure of at least 10 years.

## Alternate Designs

There are many topologies available for the DC/DC converter. There are designs for higher and lower output voltages along with inverting voltage polarity. Listed below are several topologies that will not accommodate the needs of a high voltage output. The following topologies listed below are single stage converters. Single stage converters do not have isolation between the input and output, and do not invert voltages.

### Fly-back Converter

The advantage to the fly-back converter is that it allows an output voltage of 400V DC, as required for this design. This DC/DC converter provides isolation between the input and output. However, the fly-back converter uses one switch, which will result in high heat loss. The input current for the fly-back converter is

$$I_{L_m} = \frac{V_o^2}{V_s DR}$$

where D is the duty ratio,  $V_o$  is the output voltage,  $V_s$  is the source voltage, and R is a resistance of  $32\Omega$ . The input current is approximately 365A rms for a 21V input source with a duty ratio of 0.46. Using the 365A current and the 21V input voltage, the input power is calculated as 7.7kW. Since the output power is 5kW, the efficiency can be calculated as:

$$h = \frac{P_{out}}{P_{in}} = \frac{5kW}{7.7kW} = 0.65$$

The efficiency is 65 percent, which is not a suitable design for a high voltage output. This topology is mainly used for low power applications between 1-10W, therefore is unsuitable for this project.

### Boost Converter

Another design is the Boost converter. This converter is capable of providing the 400V DC output required for the DC/DC converter however it contains only one switch which will result in poor efficiency. This will be seen through the high current that will flow in the output side. The output relationship is

$$V_o = \frac{V_s}{1 - D}$$

For a 400V output and 29V nominal input, the duty ratio would be approximately 0.9275, which means the switches will be on most of the time. The efficiency of the non-ideal switches will decrease to about 20 percent. The current through the inductor will be close



to 239A. This would result in purchasing a physically large inductor with large gauge wire to accommodate the capacity of current. This topology does not provide isolation from the input and output which is one of the design requirements of the FEC regulations.

### **C'uk Converter**

The C'uk converter is capable of meeting the demands of supplying 400V DC at the output, however to meet this goal, large size inductors need to be used. This converter has similar problems as the Boost converter because the duty ratio is too large. The duty ratio can be calculated using the following equation:

$$\frac{V_o}{V_s} = \left( \frac{D}{1-D} \right)$$

To calculate the duty ratio, a 400V output voltage and a 21V input voltage were used. The duty ratio is approximately 0.95 which causes a high switching power loss. This topology is ideal for lower power applications with lower voltage ratios, but not suitable in this design. It also does not provide isolation from the input and output which will not meet one of the design requirements.

## Alternate Designs (cont'd)

Listed below are other topologies that can be used for higher power outputs but were not chosen for the given reasons. The following topologies have a multistage operation. The multistage converter first inverts the signal to AC for use with a transformer, and then it converts back to DC voltage. By using a high-frequency transformer it provides an efficient way to step up the voltage. The transformer uses different grounds, which allows both sides of the system to be electrically isolated. This line isolation provides continuous noise filtering from the noisy primary side signal. This noise filtering allows the reduction in the electrical noise emitted in high frequency circuits.

### Push-Pull Converter

One possible topology is the Push-Pull converter. It has a configuration similar to the Full-Bridge but has two switches instead of four to cause a low switching loss. The transformer has an input and output center tap, which makes it a more difficult design to implement and hence, results in a higher cost. The transformer will need larger windings on the primary side, which will increase the physical size and weight. The output voltage relation of this converter is shown below.

$$V_{out} = 2V_{in} \left( \frac{N_s}{N_p} \right) D$$

where D is the duty cycle,  $N_p$  and  $N_s$  are the turns of the primary and secondary windings of the transformer, respectively. With the lowest input of 21V and a steady output of 400V, the duty cycle D is approximately 0.43. The output inductance can be determined by the following equation.

$$\Delta i_{L_2} = \frac{V_o \left( \frac{1}{2} - D \right) T}{L_2} \Rightarrow L_2 = \frac{400 \left( \frac{1}{2} - 0.43 \right) \times 50 \text{ } \mu\text{s}}{0.125} = 89.3 \text{ } \mu\text{H}$$

The output inductance would need to be very large, which is not practical to implement into the design.

Another disadvantage is that the MOSFETs may conduct simultaneously causing a short in the control circuit. According to performance analysis conducted on this topology, the push-pull converter is highly efficient and has fewer switches, however the transient response would be poor and the transformer would be hard to manufacture in the design.

## Half-Bridge Converter

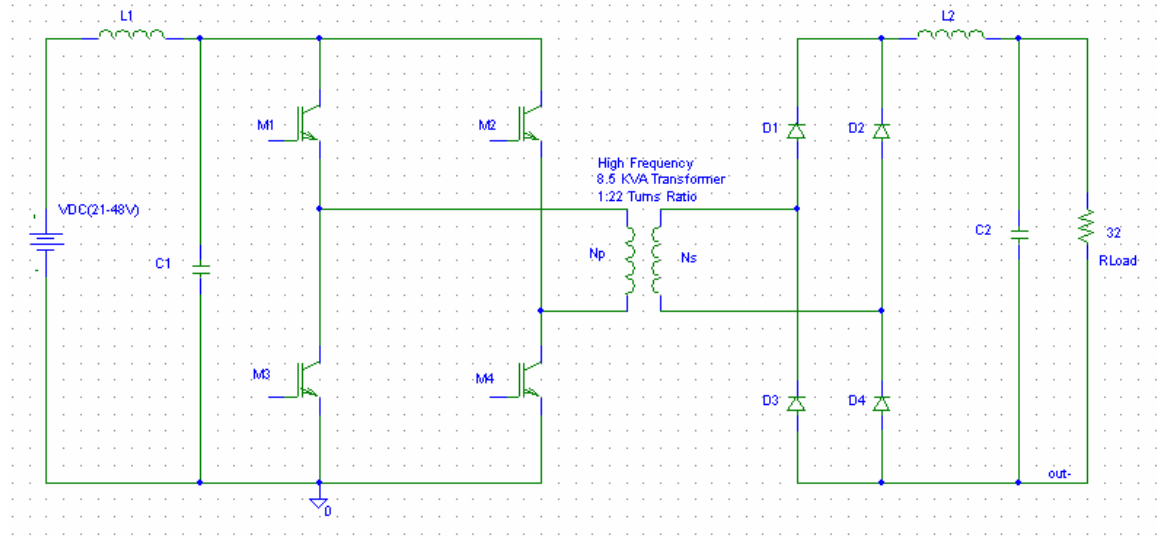
Another configuration is the Half-Bridge Converter. It has a higher efficiency and a simpler structure with only two switches. Furthermore, the output voltage of the Half-Bridge converter is half that of the Push-Pull Converter. The main disadvantage with this design is the sensitivity to the load variations. This converter will need a more complex control circuit to accommodate the rapid change of the voltage ratio. The regulated output voltage would be very difficult to control within desired constraints. The equation for the output voltage is shown below.

$$V_{out} = V_{in} \left( \frac{N_s}{N_p} \right) D$$

The duty cycle is close to 0.84, which will cause larger switching losses for the required voltage ratio. Furthermore, this topology is not suitable due to the large changes in current. For the range of input voltage (21V - 48V), the current will vary from approximately 264.52A to 115.73A, respectively. It is also harder to keep the circuit symmetrical which causes a more complex control circuit. For these reasons, this topology is unsuitable for this application.

## Accepted Technical Design

The accepted topology for this project is the Full-Bridge DC/DC converter shown in Figure 1.



**Figure 1. Full-Bridge DC/DC Converter**

The Full-Bridge DC/DC converter will have to maintain a constant 400V DC output with a varying 21-48V DC (29V DC nominal) input. This is accomplished by using Pulse Width Modulation (PWM) control. By increasing or decreasing the duty cycle (D) of the square-wave pulses to the switches M1-M4, the output voltage can be held constant with a varying input voltage. The output voltage can be calculated as follows:

$$V_{out} = \frac{2}{T} \int_0^t \frac{V_{in}}{\left(\frac{N_p}{N_s}\right)} dt$$

where: T is the switching time or the inverse of the frequency  $\left(\frac{1}{f}\right)$ ,  $\left(\frac{N_p}{N_s}\right)$  is the transformer turns ratio, and (t) is the pulse width time.

Solving for t:

$$t = \frac{V_{out} N_p T}{2V_{in} N_s}$$

$$\text{Duty Cycle (D)} = \frac{t}{T}$$

The Full-Bridge DC/DC converter topology was chosen for several reasons. The primary benefit of using a Full-Bridge DC/DC converter is its power handling capabilities, stability, and symmetry. Secondly, using a high frequency transformer is one of the most efficient ways to step up the voltage and to transfer the 5 kW of power to the full-wave rectifier circuit. The high frequency transformer is also much smaller and lighter than a standard 8.5 kVA 60 Hz transformer.

The input power for a 5 kW Full-Bridge DC/DC converter with 90 percent efficiency is calculated as follows:

$$P_{in} = \frac{P_{out}}{h} = \frac{5kW}{.90} = 5.55kW$$

With knowledge of the input power, the worst-case input current (21V input) can be calculated as follows:

$$I_{worst} = \frac{P_{in}}{V_{worst}} = \frac{5.55kW}{21V} = 265A$$

It will be important to choose a switch that can efficiently handle the significantly high current. For this type of application, there are two types of switches to choose from, one being the Insulated Gate Bipolar Transistor (IGBT), and the other a Metal Oxide Semiconductor Field Effect Transistor (MOSFET). They both have advantages and disadvantages. IGBTs typically are used in applications for switching frequencies less than 20 kHz, high-voltage applications (>1000V), and high temperature situations (>100°C). MOSFETs are typically used for applications of high switching frequencies, low-voltage applications (<250V), and lower temperature situations. The IGBT's conduction losses are higher than a MOSFET's conduction losses at lower temperatures, thus making it more efficient in the long run for low temperature applications. The MOSFET switch was chosen for the Full-Bridge DC/DC converter since it will be utilized in a low voltage application (21-48V) and a low temperature situation. Temperature will be maintained with the implementation of cooling devices such as fans and heat sinks.

To minimize switching losses 5 or 6 MOSFETs will be placed in parallel for each switch. A typical MOSFET will have a static on-state resistance of approximately 10mΩ. The static on-state resistance for one switch with 6 MOSFETs in parallel will be approximately 1.66mΩ. Taking the worst-case input current and the static on-state resistance of the MOSFET into consideration, the worst case switching power losses can be calculated as follows:

$$P_{mosfet\_switchinglosses} = 2I^2R_{on} = 2 \cdot 265^2 \cdot 1.66m\Omega = 233W$$

After inverting the DC input voltage into an AC voltage, an efficient way to step up the voltage is necessary. The high frequency transformer was specially designed for 20 kHz

applications, which minimized hysteresis losses. This made it approximately 98% efficient. The power loss of the high frequency transformer can be calculated as follows:

$$P_{loss\_transformer} = P_{in\_transformer} (1 - \eta) = (5555 - 233)(1 - .98) = 106W$$

The high frequency transformer isolates the input from the output, a requirement of the FEC competition. Given the availability of the 20 kHz transformer, the design will implement this transformer, thus saving the DC/DC converter team approximately \$800 in material costs.

To convert the AC voltage from the secondary terminal of the transformer to a DC voltage, a full-wave rectifier configuration was chosen. The full-wave rectifier configuration will produce a higher average voltage than a half-wave rectifier. To determine the switching losses of the diodes, the output current and switching resistance of the diodes must be calculated. The output current is calculated as shown below:

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{5kW}{400V} = 12.5A$$

The switching resistance of the diodes is approximately 0.1Ω per diode. The diode switching losses can then be calculated as follows:

$$P_{loss\_diodes} = 2 \cdot I^2 R_{on} = 2 \cdot 12.5^2 \cdot 0.1\Omega = 31.25W$$

After calculation all of the individual losses, the total power losses and overall efficiency can be determined. Since the controls circuit is mostly comprised of circuitry that consumes very little power, their power losses will be neglected. The following equation calculates the total losses of the Full-Bridge DC/DC converter neglecting power losses from the control circuit.

$$P_{loss\_total} = P_{loss\_mosfets} + P_{loss\_transformer} + P_{loss\_diodes} = 233W + 106W + 31.25 = 370.25W$$

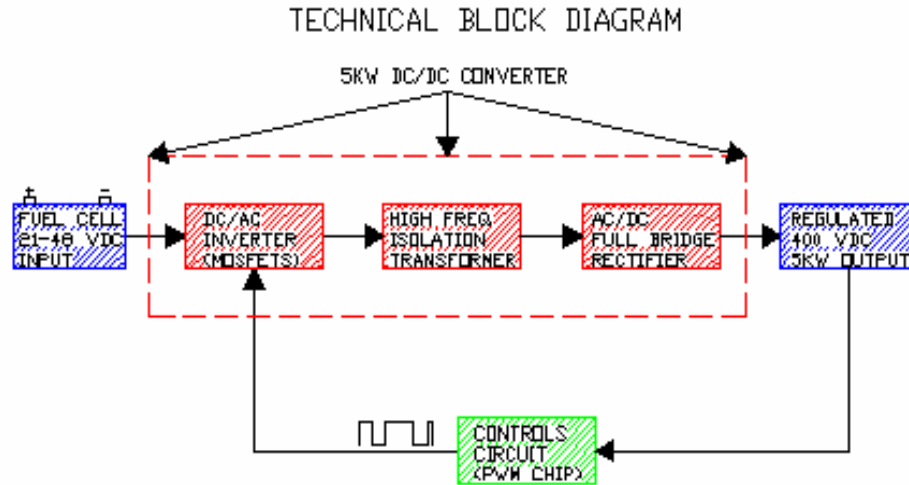
The overall efficiency is approximated as follows:

$$\eta_{overall} = \frac{P_{out}}{P_{out} + P_{loss\_total}} \cdot 100\% = \frac{5kW}{5kW + 370.25} \cdot 100\% = 93.1\%$$

The overall efficiency of 93.1 percent is based on worst-case conditions with a duty cycle of 0.45. The duty cycle will decrease as the input voltage increases from 21 volts. A lower duty cycle will result in a higher efficiency with lower switching power loss. This will meet the design requirements stated earlier of a minimum 90% efficiency. The Full-Bridge DC/DC converter will be the efficient and practical choice for the application and design requirements of the DC/DC converter. The final product will be required to fit in a box with a volume of 1.5<sup>3</sup> cu-ft, a requirement of the FEC competition. This design

will need no additional source to attain the 400V output. The user will simply apply a 21 - 48V source on the input end of the product to receive the desired voltage and power.

The technical block diagram shown below in Figure 2 shows the complete system setup.



**Figure 2. Technical Block Diagram of Complete System**

Using several 12V lead acid batteries, which will be connected in various configurations to vary the input voltage, will simulate the fuel cell shown in Figure 2. The reason for using lead acid batteries versus using a variable DC input from the Energy Conversion Laboratory is that a DC power source in the Energy Conversion Laboratory cannot supply the amount of current needed for the 24V test, which was stated earlier at 265A.

There will be three varying input voltage tests done on the DC/DC Converter to verify that it can regulate a 400V output regardless of the input voltage. The three voltages used to simulate a varying fuel cell input voltage will be 24V, 36V, and 48V. Since the batteries produce 12V each, these are the only testing levels for any given configuration.

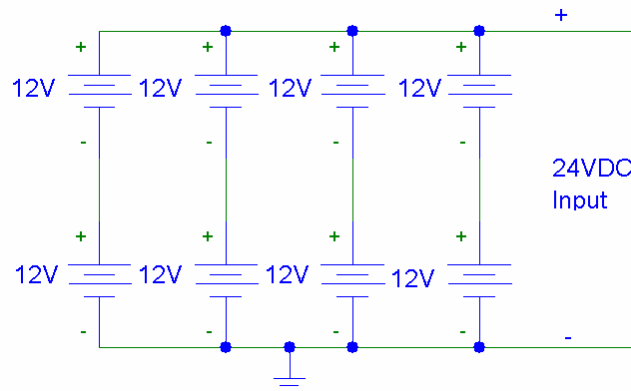
Exide Technologies manufactures the batteries used to supply the varying DC input voltage for this project. The batteries, model number NG-27, are marine deep cycle 12V batteries. Table 1 shown on the next page, shows the nameplate data of the batteries being used to supply the varying DC input voltage. The MCA rating refers to the Marine Cold Amps, which is the amount of current the battery can deliver for 30 seconds at 32 degrees Fahrenheit while maintaining a constant voltage of 1.2V per cell. The next rating CCA, which means Cold Cranking Amps, is the amount of current the battery can deliver for 30 seconds at 0 degrees Fahrenheit while maintaining a constant voltage of 1.2V per cell. RC, the reserve capacity, is the amount of time the battery can deliver 25 Amps at 80 degrees Fahrenheit while maintaining a constant voltage of 1.75V per cell. The final rating is the AMP/HR rating, which is the amount of current the battery can deliver for

one hour. For example, if a battery can deliver 25A for 5 hours, the battery would have an AMP/HR rating of 125AMP/HR.

MCA	625
CCA	500
RC	180
AMP/HR	105

**Table 1. NG-27 Manufacturer Ratings**

Using the nameplate data from the batteries the connection configurations for the batteries can be designed. For the 24V test, the batteries will have to be able to deliver 265A. The Figure 3 shown below shows the connection diagram for the batteries of the 24V test.



**Figure 3. 24V DC Input Connection Diagram**

For a series connection the total output voltage changes but the total AMP/HR remains the same. When connected in parallel, the AMP/HR are summed together but the voltage remains the same. For the circuit shown in Figure 3 the total AMP/HR would be 4 times 105 AMP/HR, which equals 420 AMP/HR of capacity. The following equation shows how to calculate the theoretical operating time that the batteries should be able to deliver the rated current.

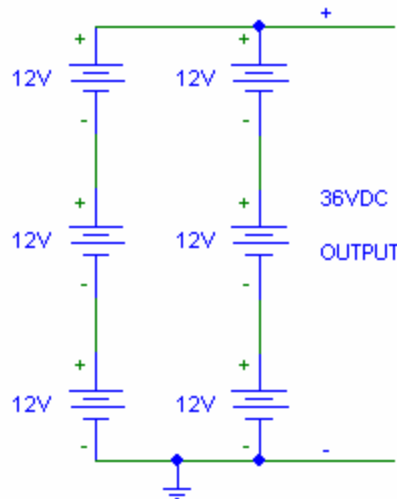
$$Time = \frac{AMP / HR}{Current} = \frac{420AMP / HR}{265Amps} = 1.58Hours$$

The next test will be for 36V. The first step to designing the battery connection for this test is to calculate the current for the 36V test. This is calculated by using the equation shown on the next page. For simplicity, the input power will be assumed to be the same as the worst-case power input stated earlier in the report at 5.55kW.

$$I_{input} = \frac{P_{in}}{V_{in}} = \frac{5.55kW}{36V} = 154A$$



Figure 4 shown below, shows the connection diagram for the 36V test. This connection will provide 210 AMP/HR capacity, and will deliver 154A for approximately 1.36 Hours.



**Figure 4. 36V Battery Connection Diagram**

The final test is for 48V. As with both the 24V and 36V test the current must be calculated to determine how the batteries should be connected. The input current for the 48V test is calculated using the equation shown below.

$$I_{input} = \frac{P_{in}}{V_{in}} = \frac{5.55kW}{48V} = 116A$$

Figure 5 shown on the next page shows the battery connection diagram for the 48V test. The connection shown will provide 210 AMP/HR of capacity, and will deliver 116A of current for approximately 1.81 Hours.

For the input voltage supply, a capacitor  $C_1$  and inductor  $L_1$  filter must be determined. This will keep the supply regulated at the designated value. The capacitor for the input is based on the extreme case where the voltage is 21V and the current is at maximum (265A). The  $I_{rms}$  for the input is calculated.

$$I_{rms} = \frac{I_{in}}{2 \cdot D} = \frac{265A}{2(0.45)} = 294.44A$$

With this value, the current through the capacitor is shown as

$$I_{cap} = \sqrt{(I_{rms}^2 - I_{in}^2)} = \sqrt{(294.44^2 - 265^2)} = 128.34A$$

The capacitor is determined to be:

$$C_1 = \frac{I_{cap}}{w \cdot \Delta V} = \frac{128.34A}{(2 \cdot p \cdot 20 \cdot 10^3) \cdot 0.21} = 4.863mF$$

where  $\Delta V$  is the percent ripple. It is determined as  $\Delta V=(21V)(.01)$  with 1% ripple factor. The capacitor  $C_1$  is shown in Figure 1.

The input inductance  $L_1$  is chosen to be very small based on the fact that the input voltage source will be pure DC. An inductance of 10nH will suffice for this use, but not for sources other than a pure DC.

The inductance  $L_2$  and capacitance  $C_2$  values on the output side are to be determined for a ripple of less than 1%. With a duty cycle of 0.45 and load resistance of  $32\Omega$ , the critical inductance is calculated below.

$$L_{crit} = \frac{1-D}{4} \cdot R \cdot T = \frac{1-0.45}{2(0.45)} \cdot \frac{32}{20k} = 220.0mH$$

where T, D, and R are the period, duty ratio, load resistance respectively. The output inductance is desired to be

$$L_2 \geq 10 \cdot L_{crit} = 2.20mH$$

That value will help determine the minimum capacitance for the filter system of the rectified DC voltage. The capacitance is shown as

$$\frac{\Delta V_o}{V_o} = \frac{1-D}{8 \cdot L_2 \cdot C_2 (2f)^2} \Rightarrow 0.01 = \frac{1-0.45}{8(0.00228)C_2 (2 \cdot 20000)^2} \Rightarrow C_2 > 2mF$$

where  $L_2$ ,  $C_2$ ,  $f$  are the output inductance, output capacitance, and frequency respectively. Since the minimum value must be 2 mF, the chosen value will be 10 mF for a better filter system. These values are tentative based on calculations and simulations. They may need to be adjusted for a better performance. All of the components  $C_1$ ,  $L_1$ ,  $C_2$ ,  $L_2$  can be seen in Figure 1.

The next part of the technical block diagram shown in Figure 2 is the DC/AC inverter. The DC/AC inverter being used for this DC/DC converter will use several MOSFETs that will be connected in parallel to handle the high current. The MOSFET that has been chosen for this project is the IRFPS3810, which is manufactured by International Rectifier. The IRFPS3810 was chosen because of its low static on-state resistance of  $9m\Omega$ , and its high current handling capabilities. For the IRFPS3810 the drain is shared with one of the legs of the MOSFET and the backside of the MOSFET. Therefore, three heat sinks will be needed, since the two high side MOSFETS share the same drain. For

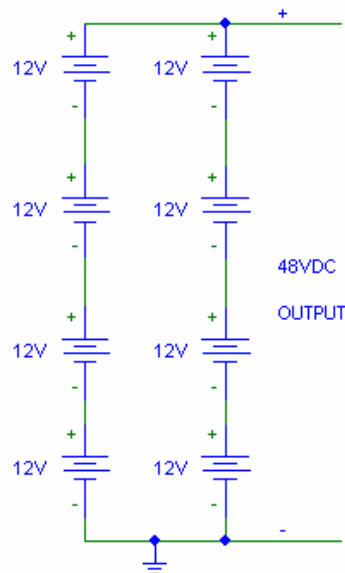
the low side, two individual heat sinks will be sufficient. All of the wire connectors are rated at 75° C and will be working in an ambient temperature of 30° C. Therefore, the thermal resistance calculation of the designated heat sink is shown below.

$$Q = \frac{\Delta T}{R} \rightarrow R = \frac{\Delta T}{Q} = \frac{(75 - 30)}{(233W/2)} = 0.38^{\circ}C/W$$

where Q is the power dissipated, ΔT is the change in temperature of a maximum of 75° and R is the thermal resistance.

The thermal resistance of the heat sink for the MOSFETS should be below 0.38° C/W in order to keep the MOSFETS temperature below 75° C. The calculation for the thermal resistance of the heat sink for the diodes is shown.

$$Q = \frac{\Delta T}{R} \rightarrow R = \frac{\Delta T}{Q} = \frac{\Delta T}{2(I_{diode}^2 \cdot R_{diode})} = \frac{(75^{\circ} - 30^{\circ})}{2(12.5^2 \cdot 0.1)} = 1.44^{\circ}C/W$$



**Figure 5. 48V Battery Connection Diagram**

The controls circuit is the next stage of the technical diagram shown in Figure 2. This circuit is primarily composed of three integrated circuits (IC's), the UC3825BN, ISO124, and the IR2110. The UC3825BN IC, which is manufactured by Texas Instruments, is a high-speed pulse width modulation (PWM) controller. The UC3825BN is considered the central processor of the entire DC/DC converter. The UC3825BN was chosen for this project because of its compatibility with Voltage and Current-Mode topologies, and it has dual alternating outputs. The controls schematic is shown in Figure 6.

The first step in designing the controls circuit is to set both the switching frequency of the MOSFETS and the maximum duty cycle. Using the Texas Instrument specification sheets, the resistor (RT) and capacitor (CT) values can be calculated using the following equation.

$$CT = \frac{(1.6 \cdot D_{MAX})}{RT \cdot f}$$

Texas Instruments recommends using RT values ranging from 1kΩ to 100kΩ. The switching frequency was stated earlier at 20kHz, and the maximum duty cycle was chosen to be 0.45. Choosing RT to be 1.5kΩ, the capacitor value (CT) was calculated to be 0.022μF, which is a commonly manufactured capacitor. A 5kΩ potentiometer (P2) will be used in place of RT, so that the control circuit can be adjusted to switch at a frequency close to 20kHz.

The UC3825NB PWM chip adjusts the duty cycle of the high and low side outputs to the IR2110 drivers achieving the 400VDC output. The 400VDC output voltage is monitored using the ISO124 chip. The ISO124 chip provides isolation from the output and the input circuits. The voltage divider circuit consisting of resistors R8 and P4 will set the desired value for VIN (pin 27) of the ISO124 chip to 5.1V. The 5.1V is then isolated and transferred to VOUT (pin 13) of the ISO124 chip, which is sent to IN- (pin1) of the PWM chip. The resistor R5 acts as a buffer resistor between the two chips; R5 absorbs the residual voltage if the voltage to IN- goes above 6.8V (Zener diode). The PWM chip then references its own 5.1V from pin 16. If IN- (pin1) is lower than 5.1V the PWM chip will adjust the duty cycle to keep the voltage regulated at the desired voltage. If the voltage to IN- (pin 1) is higher than 5.1V the PWM chip will shut off the two outputs (pins 11,14).

The UC3825BN PWM chip also monitors the input current to the DC/DC converter. Using a 2000:1 current transformer this can be accomplished. With a maximum input current of 265A, the current at the secondary of the current transformer will be 0.132A. To create 5.1V, a potentiometer (P3) set at 37.5Ω is placed in parallel with the secondary of the current transformer. A voltage divider circuit consisting of R3 and P3 is used to create a voltage of 1V, which goes to ILIM (pin 9). If the voltage at ILIM goes above 1V the PWM chip will shut off the two outputs (pins 11,14).

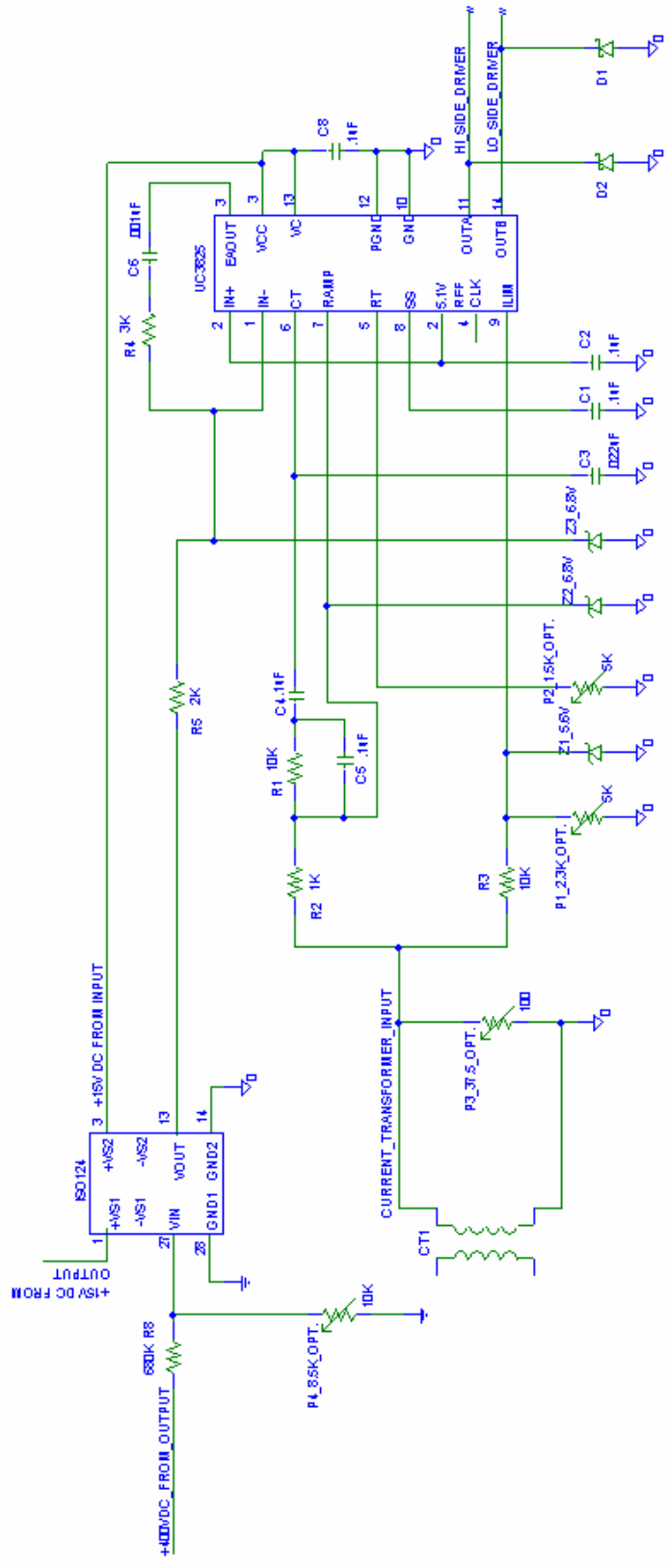
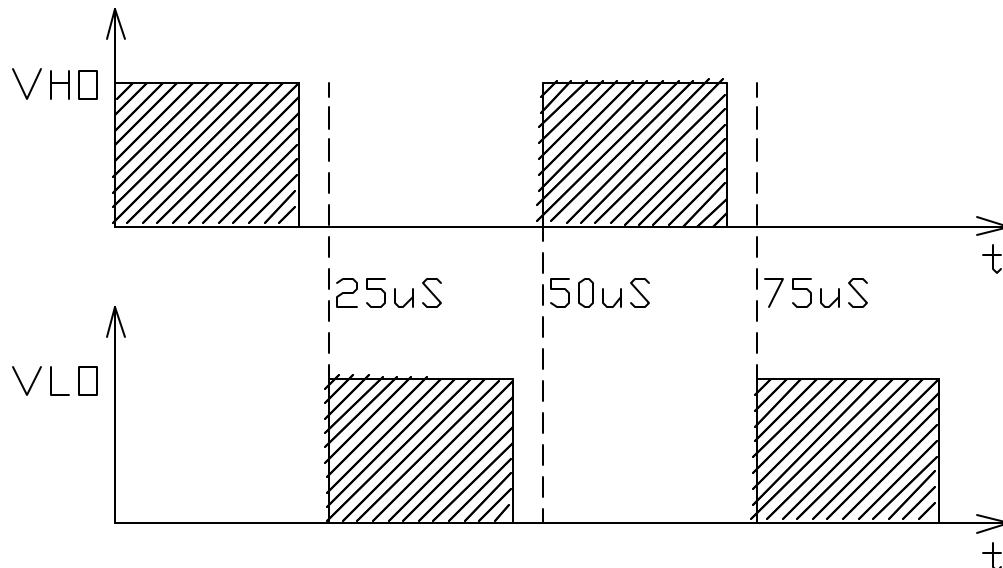


Figure 6. Controls Circuit Schematic

When the RAMP (pin 7) is connected to the timing capacitor (CT) the UC3825BN acts as a duty cycle control IC. The RAMP (pin 7) is also connected to a slope compensation circuit consisting of two resistors and two capacitors (R1,R2,C4,C5). The two resistors (R1,R2) act as a voltage divider between the oscillator output and the RAMP. Capacitor C4 is an AC coupling capacitor, and capacitor C5 filters the noise of the current waveform reducing any parasitic capacitance. Resistor R4 and capacitor C6 control the output gain of the PWM chip, these values may have to be adjusted once the controls circuit is being tested.

Capacitors C1, C2, and C8 were chosen and placed into the circuit as shown, based on Texas Instruments recommendations from the specification sheets. The Zener diodes Z1, Z2, and Z3 were chosen due to the maximum voltage constraints to the pins of the PWM chip. For pins 1 and 7 the maximum voltage to both pins cannot exceed 7V, therefore, to be safe, a 6.8V Zener diode was picked to ensure the voltage to the pins would never exceed 7V. For pin 9, a 5.6V Zener diode was picked since the maximum voltage to the pin cannot exceed 6V per the specifications of Texas Instruments. The Schottky diodes (D1, D2) will prevent ringing below ground, these are connected to the output pins (11, 14). The Schottky diodes will also damp any parasitic inductive kicks from the gates of the MOSFETS.

The next part of the controls circuit is the gate driver circuit. The outputs of the UC3825BN chip are alternately controlled. When one output is on, the other output is off. Each output switches at one half the frequency (20kHz), which is every 25 $\mu$ S. Figure 7 shown below, illustrates how the outputs of the PWM chip work. The outputs shown below in Figure 7 are for the 24V test, with a duty cycle of approximately 0.43.



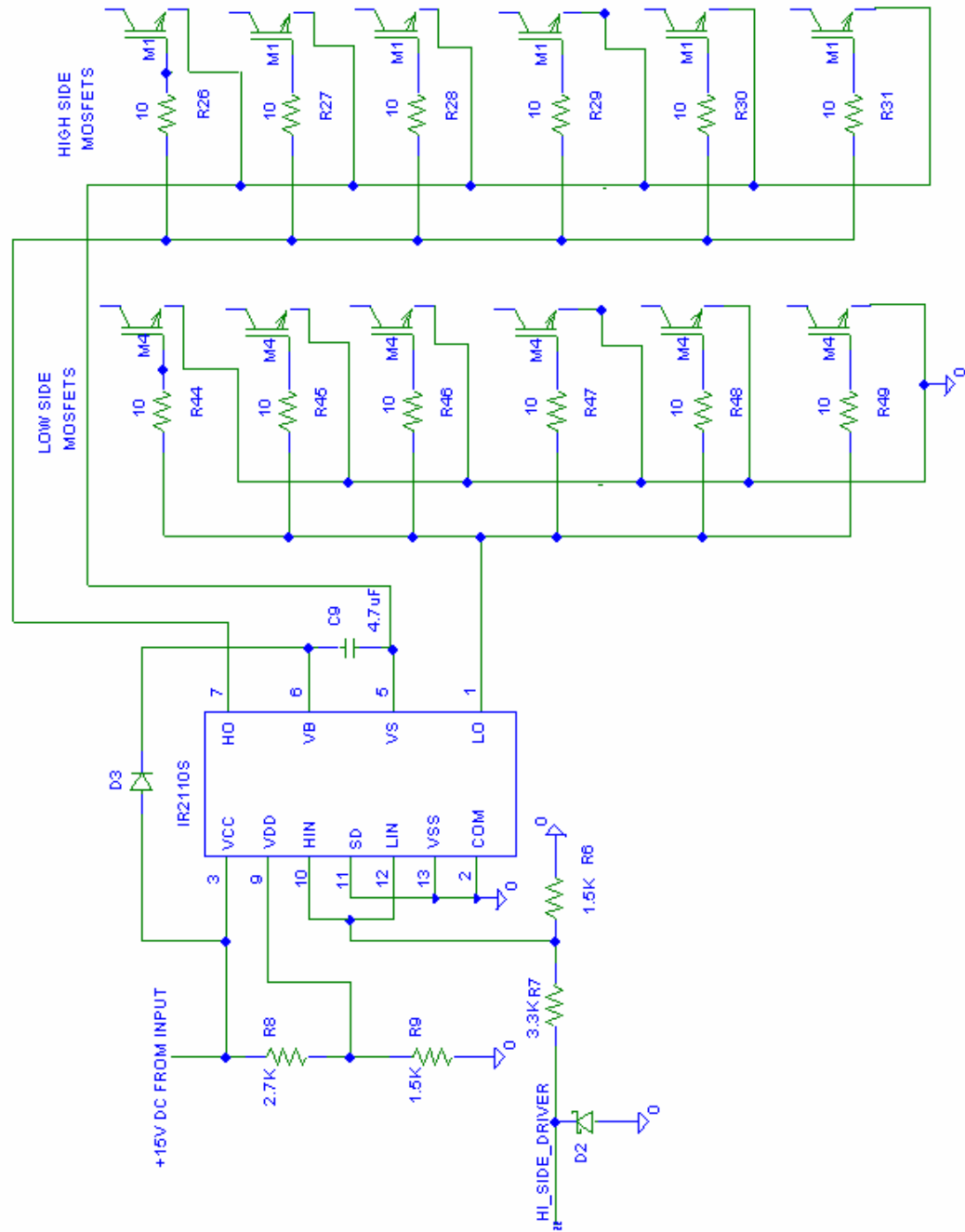
**Figure 7. Outputs of the UC3825NB for Duty Cycle of 0.43**

For this controls circuit there are two IR2110 gate drivers. International Rectifier manufactures the IR2110 gate driver IC. This gate driver IC was chosen because it has

independent high and low side drivers which is needed for the inverter circuit, and its outputs are in phase with its inputs. The gate driver schematic for the IR2110's is shown in Figure 8. The gate driver schematic in Figure 8 is only for the high side driver input from pin 11 of the UC3825BN. The gate driver schematic will be the same for the low side driver input from pin 14 of the UC3825BN, which will not be shown in this report.

The input signal coming from the UC3825BN enters into a voltage divider to reduce the voltage to HIN and LIN (pins 12,14) of the IR2110 chip. The voltage divider consisting of resistors R6 and R7 will create approximately a 5V signal from the PWM chip to HIN and LIN (pins 12,14). Pins 12 and 14 are tied together since they will drive the set of MOSFETS M1 and M4, which are the set of paralleled MOSFETS that are diagonally across from each other. MOSFETS M1 and M4 need to switch at the same time. The IR2110 will provide a high and low side driver for both switches, and switch the two MOSFETS at the same time as well.

The IR2110 is powered by +15VDC to VCC (pin 3). For VDD, the voltage has to be lower than 15V so the logic levels can be recognized. A voltage divider consisting of R8 and R9 is implemented to produce 5V to VDD (pin 9).



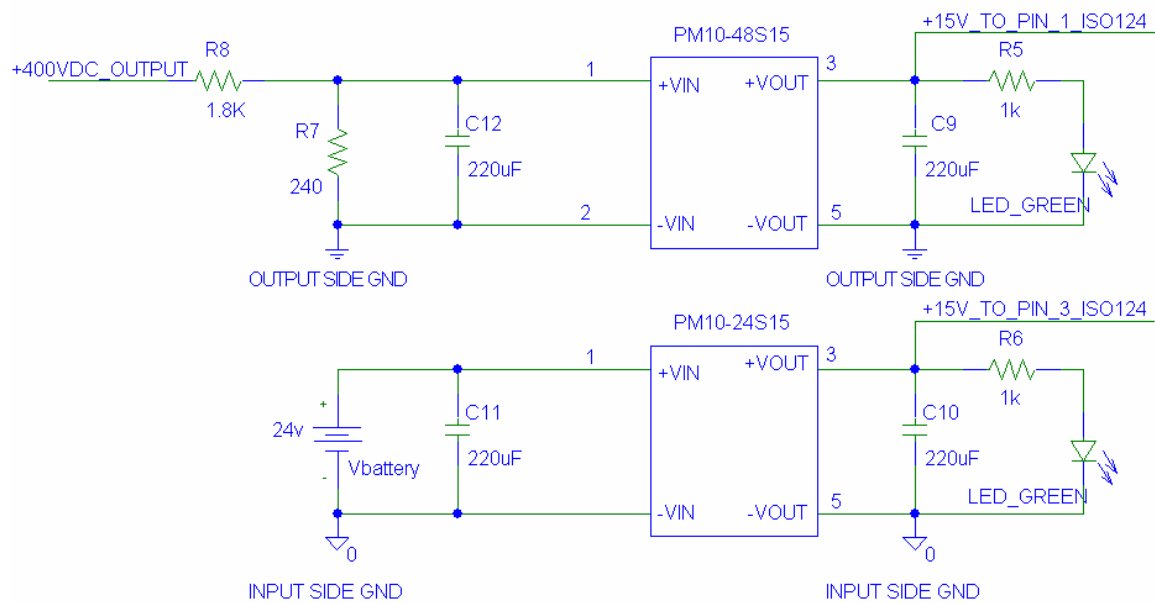
**Figure 8. Gate Driver Schematic (HI-Side Input)**

A bootstrap circuit consisting of diode D3 and capacitor C9 also has to be implemented into the gate driver circuit. The bootstrap diode (D3) needs to block the full power rail voltage, which occurs when HO (pin 7) is energized. The bootstrap diode also must have a fast recovery time to minimize the charge that regenerates from the bootstrap capacitor back into the VCC source. The bootstrap capacitor (C9) minimizes the overcharging and voltage ripple between VB and VS (pins 5,6).



To switch the high-side MOSFETS, HO (pin 7) is connected to a 10W (R26-R31) resistor that is connected to the gate of the MOSFET (6-M1), and VS (pin 5) is connected to the source of the MOSFET. For low-side switching, LO (pin 1) is connected to a 10W (R44-R49) resistors that is connected to the gate of the MOSFET (6-M4).

To provide +15V to all of the IC chips, two Lambda DC/DC converters will be used. The IC power supply schematic is shown below in Figure 9. One 24V/15V DC/DC converter, Lambda PM10-24D15, will be used to provide +15V to the UC3825BN PWM IC, the IR2110 gate driver IC's, and the ISO124 isolation IC. A 48V/15V DC/DC converter, Lambda PM10-48S12, will be used to provide +15V to pin 1 of the ISO124 isolation IC.



**Figure 9. IC Power Supply Schematic**

To reduce the 400VDC output of the DC/DC converter, a voltage divider consisting of resistors R7 and R8 is used to produce 48VDC into the 48V/15V DC/DC Lambda converter. 24V will be supplied to the Lambda 24V/15V DC/DC converter by directly connecting it to the batteries. The capacitors (C9-C12) are used to provide filtering. A green Light Emitting Diode (LED) will be used on both Lambda DC/DC converters to indicate they are both producing +15V and will help save time in troubleshooting.

Another important design issue is the proper sizing of wire, circuit breakers, and fuses. If the wire, circuit breakers, and fuses are not sized properly there runs a risk of fire and possible human electrical shock. To aid in the designing of the wire size, circuit breakers and fuses, the National Electric Code (NEC) handbook will be consulted.

The first step is to design the wire size from the batteries. As stated earlier, the maximum worst case current that will be fed from the batteries is approximately 265A. According

to Table 310-16 of the NEC, 1/0 Thermoplastic (T) 90° C (HH) Nylon Outer Jacket Material (N) wire, also known as THHN wire, is capable of handling 150A at 75° C. The 75° C column is used instead of the 90° C column because of Article 110-14C in the NEC handbook. Article 110-14C states that the temperature rating of the conductor shall not exceed the lowest temperature rating of the termination device(s). A majority of termination devices are rated at 75° C, therefore the 75° C wire column was chosen when designing the wire sizes. Paralleling two 1/0 THHN wires will have a combined current handling capability of 300A. Table 310-15B2A of the NEC does not require any adjustment factors for two 1/0 THHN conductors since there are no more than three current carrying conductors for the circuit.

The next step is to design the wire size for the individual branches of the MOSFETS. For worst case, there will be 265A of current entering each branch of the MOSFETS. Since there will be six MOSFETS being used per branch there will be approximately 44A of current going through each MOSFET. The six individual wires will be bundled together to save space, therefore the wires will have to be de-rated 80% and still have a current handling capability of 44A according to Table 310-15B2A of the NEC. In other words, the wire will have to have a current handling capability of 53A. Using Table 310-16 of the NEC # 6 THHN wire has a current rating of 65A. On the other hand, # 8 THHN wire could have been used if de-rating was not an issue.

The output circuit wires need to be designed as well. The average current flowing through the diodes (output circuit) will be approximately 12.5A. Number 14 THHN wire has a current rating of 20A according to Table 310-16 of the NEC handbook. However, the handbook states that it cannot be used for 20A circuits, it can only be used for 15A circuits. To avoid the possibility of blown fuses, a 20A fuse will be implemented in the output circuit. This means that #12 THHN wire will be needed instead of # 14 THHN wire. Table 310-16 states that #12 THHN wire is rated for 20A circuits, therefore this wire will be used for the output circuit.

After sizing the wires, the circuit breaker for the batteries can be sized. Circuit breakers will provide over current protection for the wires and components of the DC/DC converter. Considering the worst-case input current of 265A the circuit breaker can be chosen. Article 240-6A of the NEC shows the standard values for circuit breakers. 265A falls between the standard circuit breaker sizes of 250A and 300A, which creates a problem when designing the correct circuit breaker size. However, Article 240-3B of the NEC allows the next higher size circuit breaker to be chosen even if it exceeds the current rating of the wire being protected. Therefore, a 300A circuit breaker will be used to provide the over-current protection of the DC/DC converter. There will be no need to de-rate the circuit breaker 80% since the operating time of the load will be no longer than 1.81 hours. This will be classified as a non-continuous load according to the definition of continuous load in the NEC. A continuous load is defined in Article 100 of the NEC handbook, which defines a continuous load when the maximum current remains on for longer than a period of three hours.

With the completed circuit, the most challenging problem will be the electromagnetic interference (EMI). The space constraint that must be followed in order to make the package comply with the FEC specifications is difficult. The switching that occurs at such high currents and frequencies will generate large EMI fields that will permeate to the other components in the system, creating large amounts of electrical noise. Another major contributor to noise in the system will be the current carrying conductors, which will be carrying large current. Parasitic capacitances will play a partial contribution to the noise in the system. Efforts will be taken to circumvent these problems; first the components will have to be strategically placed so that any EMI that is not contained by shielding will have minimal effect on the rest of the system. Due to the space constraints this will be the most arduous task. Secondly for the conductors, all forward and return paths must be kept as close as possible to one another so that the generated fields will nullify one another. Finally, to minimize parasitic capacitances and aid in the above EMI issues wire lengths will be kept as little as possible.

The following table lists the parts required for the DC/DC converter. The Refdes column references the part numbers used in the schematics. The Part Num. column contains the part numbers/names given by the manufacturers. Some of these components are readily available from the university, whereas others must be ordered through their respective vendors.

**Table 2 – Parts List**

Qty.	Refdes	Part Num.	Description
1	U1	UC3825BN	T.I. High Speed PWM Controller
1	U2	ISO124U	OPTO-Isolator (28 SOIC)
2	U3,U4	IR2110S	MOSFET Driver High/Low (16 SOIC)
2	U5	PM10-48S15	Lambda 48V-15V DC/DC Converter
2	U6	PM10-24S15	Lambda 24V-15V DC/DC Converter
30	M1,M2,M3,M4	IRFPS3810	Power MOSFET
4	D1,D2,D3,D4	ISL9R30120G2	30A 500V rated Diode
1	R8	1.8K	1W Voltage Divider for 48V DC Conv.
1	R7	240	1/4W Voltage Divider for 48V Conv.
3	P4	10K POT	1/4W 10K Potentiometer
1	P3	100 POT	2W 100ohm Potentiometer
2	P1,P2	5K POT	1/4W Potentiometer
3	R2,R5,R6	1K	1/4W resistor
1	R8	680K	1/4W resistor
3	R6,R9	1.5K	1/4W resistor
2	R7	3.3K	1/4W resistor
1	R8	2.7K	1/4W resistor
1	R5	2K	1/4W resistor
1	R4,R7	3K	1/4W resistor
24	R44-49,R26-31	10ohm	1/4W resistor
5	C1,C2,C4,C5	.1uF	50V Ceramic Capacitor
1	C6	.001uF	50V Ceramic Capacitor
4	C9b-C12	220uF	100V Electrolytic Capacitor
6	C9a	4.7uF	50V Electrolytic Capacitor
2	C1	4.863mF	Input Capacitor Filter 75V
1	C2	>2uF	Output Capacitor Filter 500V
2	Z2,Z3	6.8V ZENER	6.8V Zener Diode Voltage Regulator
1	Z1	5.6V ZENER	5.6V Zener Diode Voltage Regulator
2	D1,D1		1A Schottky Diode
2	N/A	GREEN LED	Green led for DC/DC Converters
2	N/A		2 Diodes for IR2110
1	CT1	HTR 200-SB	Current Transformer
1	N/A	CUSTOM	8.5kVA 20kHz High Frequency Transformer
1	L1	10nH	Input Inductor
1	L2	2.28mH	Output Inductor
	N/A	WIRE	Large current carrying wire for power circuit
	N/A	CONNECTORS	Large connectors for wires
1	N/A	FUSES	20A 600V Fuse Time Delay Bussman

## Verification and Validation

First stage of verification and validation involved computer simulation of the DC/DC Converter. This stage was achieved using OrCad's PSpice simulation software. Future simulation will require the use of Math Works' Simulink, and Ansoft's Simplorer.

Before implementation of the complete DC/DC Converter, each component shall be tested thoroughly to ensure that all the parts of the system will integrate with ease. First, the transformer will be verified that it produces the required step up voltage. By inputting a voltage at the primary terminal, the transformer should step the voltage to 22 times of the input. For instance, by applying a 5V AC signal, the secondary terminals should output 110V AC signal. This test used to measure the output voltage is the open circuit test, which will be performed in the Energy Conversion Laboratory. The open circuit test is performed by applying a voltage at either the low or high side of the transformer and measuring the voltage at the other end. The terminal at the measuring end is kept open. Furthermore, the transformer should operate with approximately 98% efficiency. This can be accomplished by measuring the voltage and current at both the input and outputs. The power can be calculated using the following formula:

$$P = VI$$

where P is the power, V is the voltage and I is the current. The transformer should produce an output power that is approximately 98% of the input power.

$$h = \frac{P_{out}}{P_{in}} \times 100\%$$

The second component to be tested is the control circuit. Using the Wavetek 182 function generator in the Senior Design Laboratory, the Pulse Width Modulation chip's operation can be confirmed using the Agilent 54622D digital oscilloscope. The waveforms obtained using the digital oscilloscope will help in determining whether the PWM chip operates within the given specifications. The output voltage will be simulated with a 5.1V at the IN- pin of the UC3825BN PWM chip. The output will be measured on the low side to determine that a pulse is produced. To test the high side of the PWM chip, the IR2110 gate driver will be utilized. The low side output of the IR2110 will verify that the high side of the PWM chip produces the correct pulse. This can be achieved by connecting the digital oscilloscope at pin 1 (LO) of the IR2110 gate driver. The timing of the high side and low side pulses of the PWM chip will be measured to verify that both pulses do not trigger at the same time.

Each IR2110 gate driver will also need to be tested. An input square wave signal from the Wavetek function generator will be applied to the HIN and LIN (pins 10 and 12) of the IR2110 gate driver. The HO and LO (pins 7 and 1) of the IR2110 will be applied to two MOSFETs (please refer to figure 8 for configuration) and a LED will be connected

to the drain and source terminals of the MOSFETs. For a switching frequency of 20kHz, the LED should remain lit.

The next component for testing includes the MOSFET switching devices. Once these MOSFETs are integrated, the probe of the Agilent digital oscilloscope will be connected to the gate node to verify the signal from the IR2110. Another probe of the oscilloscope will be connected to the source to verify that each MOSFET is switching appropriately. This device will be tested using the function generator in the Senior Design Laboratory. For instance, switching times will be verified according to the given specifications from the manufacturer.

Another section of the control circuit to be tested is the ISO124 chip and the HTR 50 current transformer. With the configuration shown in figure 6, the desired values will be tested. Pin 27 and Pin 13 of the ISO124 should provide 5.1V. The 5.1V at pin 27 is supplied from the voltage divider (resistor R8) of the 400V DC output. A potentiometer will be utilized to adjust the 5.1V as needed for the ISO124. Concurrently, the current transformer will be tested to have the desired current output. As the input current fluctuates out of range, the signal to the PWM chip from the current transformer will be measured to verify that it operates within the given parameters.

The final component for testing the DC/DC converter will be to verify the efficiency of the unit. The input power will be measured and compared to the output power to ensure the overall efficiency is greater than or equal to 90 percent. Adjustments and troubleshooting may be needed in order to bring the efficiency of the unit to 90 percent or better, such as adjusting potentiometers that control the switching frequency and maximum duty cycle.

The testing of each of the individual parts of the system will allow the team to isolate a potential problem before implementation into the complete system. This is beneficial in that troubleshooting a single part of the system allows for fewer variables to affect the system rather than allowing multiple factors. After the initial testing of each individual sub-system, the next task will be integrating the circuits together to allow more troubleshooting and circuit adaptation techniques to be implemented.

## Financial Budget

The initial estimated labor cost for the DC/DC converter is \$10.00 per hour for each design team member. The breakdown of the total labor cost for each team member is as follows:

**Table 3 – Initial Labor Cost**

Design Team Member	Initial Estimate Cost
Dan Burger	\$3,200.00
Eric Dougan	\$3,200.00
Joe Oberle	\$3,200.00
Sean Periyathamby	\$3,200.00
<b>Total</b>	<b>\$12,800.00</b>

The following table outlines the initial estimate for the materials needed for a successful project. It contains the main components of the DC/DC converter. The estimate for the PWM control circuit takes into account all the components needed for the control circuit.

**Table 4 – Initial Material Cost**

Item	Initial Estimated Cost
1 – 20 kHz, 5 kVA 1:22 turns transformer	\$1,000.00
PWM Control Circuit	\$1,000.00
24 – High Power MOSFETs	\$500.00
LabVIEW Student Pricing	\$250.00
1 – High Power Inductor	\$200.00
20’ High Gauge Wire	\$200.00
Terminal Connectors	\$200.00
A/D Converter	\$200.00
Cooling Sources	\$200.00
4 – High Voltage Capacitors	\$150.00
4 – High Current Rated Diodes	\$50.00
<b>Total</b>	<b>\$3,950.00</b>

## Revised Financial Budget

The labor cost for the DC/DC converter is \$10.00 per hour for each design team member. Each semester contains 15 weeks and assuming that each individual works approximately 10 hours a week, the total amount of hours needed for a successful project is about 300 hours. The following table is the revised budget for the labor cost based on the progress of the design.

**Table 5 – Revised Labor Cost**

Design Team Member	Revised Estimate Cost
Dan Burger	\$3,000.00
Eric Dougan	\$3,000.00
Joe Oberle	\$3,000.00
Sean Periyathamby	\$3,000.00
Total	\$12,000.00

This table does not take into the account the time that each individual will spend during weekends and holidays.

The following table is the revised material cost based on a completed design and research of components needed. Some components will be donated from a previous project while some others are samples from various vendors. The prices are based on a complete price list of parts from vendor catalogs.



## Revised Financial Budget (cont'd)

**Table 6 – Revised Material Cost**

Qty.	Part Num.	Description	Unit Cost	Total Cost
1	UC3825BN	T.I. High Speed PWM Controller	\$9.24	\$9.24
1	ISO124U	OPTO-Isolator (28 SOIC)	10.33	10.33
2	IR2110S	MOSFET Driver High/Low (16 SOIC)	4.00	8.00
2	PM10-48S15	Lambda 48V-15V DC/DC Converter	47.04	94.08
2	PM10-24S15	Lambda 24V-15V DC/DC Converter	47.04	94.08
30	IRFPS3810	Power MOSFET	6.67	200.10
4	ISL9R30120G2	30A 500V rated Diode	10.62	42.48
1	1.8K	1W Voltage Divider for 48V DC Conv.	1.00	1.00
1	240	1/4W Voltage Divider for 48V Conv.	0.71	0.71
3	10K POT	1/4W 10K Potentiometer	27.37	82.11
1	100 POT	2W 100ohm Potentiometer	0.59	0.59
2	5K POT	1/4W Potentiometer	0.59	1.18
3	1K	1/4W resistor	0.37	1.11
1	680K	1/4W resistor	0.11	0.11
3	1.5K	1/4W resistor	0.11	0.32
2	3.3K	1/4W resistor	0.11	0.22
1	2.7K	1/4W resistor	0.11	0.11
1	2K	1/4W resistor	0.11	0.11
1	3K	1/4W resistor	0.11	0.11
24	10ohm	1/4W resistor	0.59	14.16
5	.1uF	50V Ceramic Capacitor	0.02	0.10
1	.001uF	50V Ceramic Capacitor	0.08	0.08
4	220uF	100V Electrolytic Capacitor	0.15	0.60
6	4.7uF	50V Electrolytic Capacitor	0.23	1.38
2	4.863mF	Input Capacitor Filter 75V	0.50	1.00
1	>2uF	Output Capacitor Filter 500V	1.00	1.00
2	6.8V ZENER	6.8V Zener Diode Voltage Regulator	0.36	0.72
1	5.6V ZENER	5.6V Zener Diode Voltage Regulator	0.36	0.36
2		1A Schottky Diode	0.14	0.28
2	GREEN LED	Green led for DC/DC Converters	0.50	1.00
2		2 Diodes for IR2110	0.50	1.00
1	HTR 200-SB	Current Transformer	50.00	50.00
1	CUSTOM	8.5kVA 20kHz High Frequency Transformer	800.00	800.00
1	10nH	Input Inductor	0.50	0.50
1	2.28mH	Output Inductor	1.42	1.42
	WIRE	Large current carrying wire for power circuit	20.00	20.00
	CONNECTORS	Large connectors for wires	20.00	20.00
1	FUSES	20A 600V Fuse Time Delay Bussman	11.13	11.13
			<b>Total</b>	<b>\$1,592.99</b>

# Project Schedule

The following Gantt chart shows the initial progress as well as the tasks that need to be completed. The tasks that have been completed have a check mark beside the task name and a black dash through the time bar. The chart shows an initial estimate of the design process amongst all the team members. It will act as a guideline for the completion of the design. The revised Gantt chart (figure 11) shows more of the sub-tasks that need to be performed for a successful project completion. Since time has passed since the last submission, more of the tasks have been completed. This is reflected by check marks placed next to the tasks that have been completed.

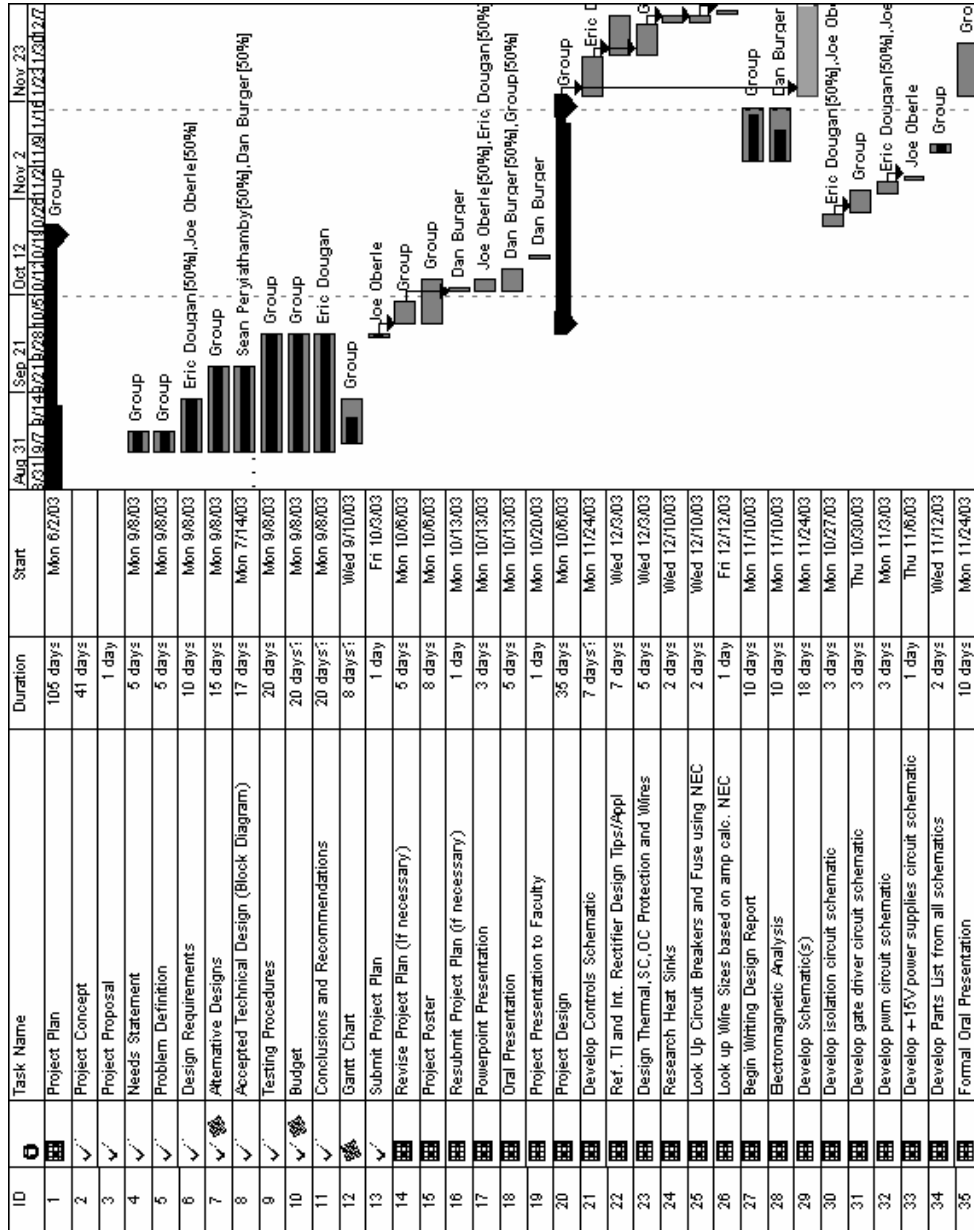


Figure 10 –Gantt chart – Design

# Revised Project Schedule

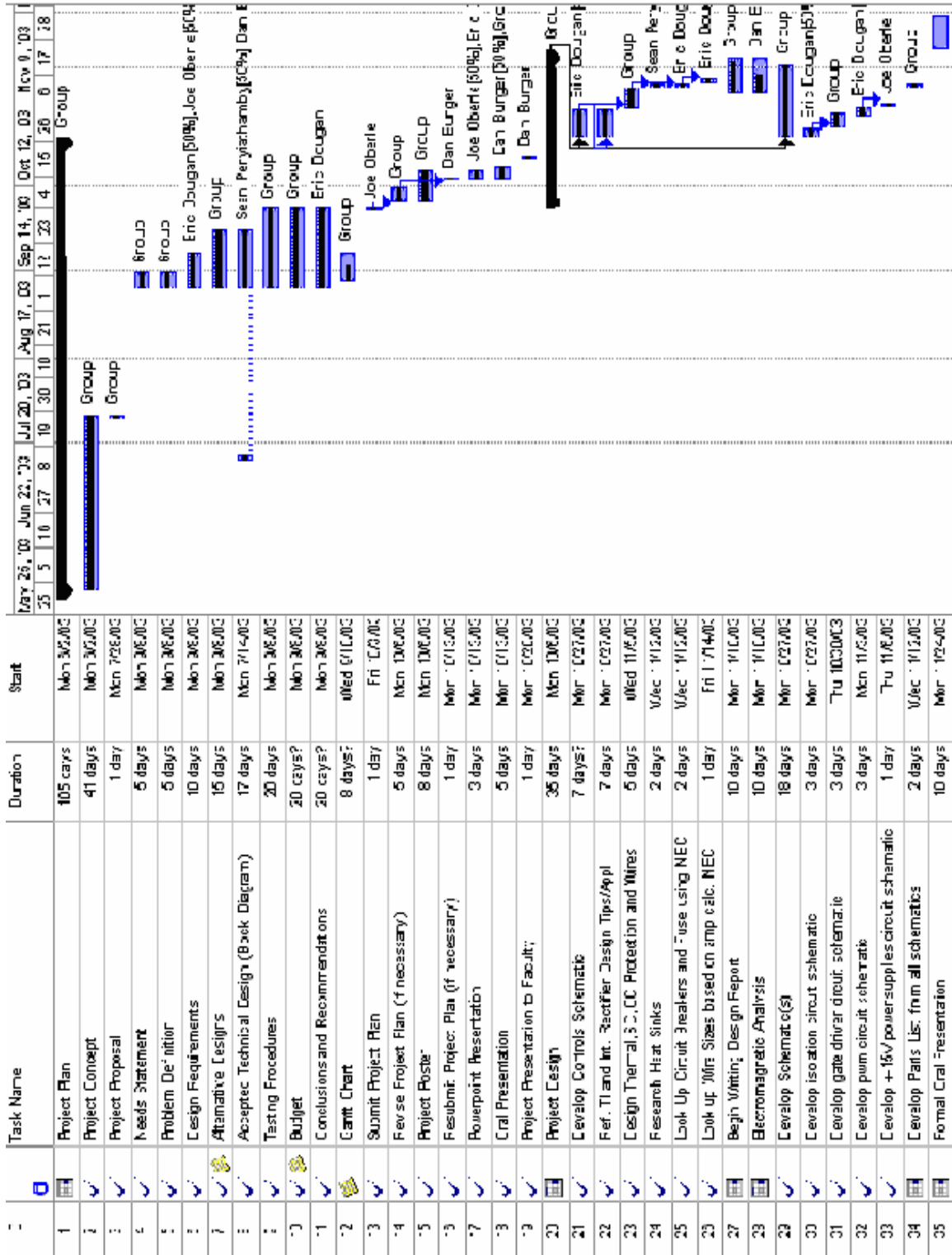


Figure 11 – Revised Gantt chart – Design

## **Design Team Information**

Dan Burger  
Electrical Engineering

Joe Oberle  
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Eric Dougan  
Electrical Engineering

Sean Periyathamby  
Electrical Engineering

## **Conclusions and Recommendations**

The team is confident that the Full-Bridge DC/DC Converter will meet the required specifications. The simulations and calculations illustrate that the Full-Bridge is the suitable topology. With the components and the control design configuration chosen, the space constraints should be satisfied. For various sections of the control circuit, the configurations were based on the manufacturers recommended connections given by the specification data sheets, applications notes, and design tips. Most of the values were calculated for the circuit specification of the full bridge converter. During implementation of the DC/DC converter, some of these may have to be adjusted to produce the desired results.

Moreover, the final product will be within the Future Energy Challenge regulations. It will be a portable module, which can be integrated with other components of the Fuel Cell Inverter. It is recommended for the FEC competition that the participating team parallel this design with an identical converter to produce the required power output. Additionally, successful completion of this design will benefit society by providing an alternate energy source especially in developing countries. The design will remain cost efficient while maintaining a long Mean Time To Failure Rate.

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## **Appendix**

### **Datasheets**

The following pages are the datasheets of the components that will be used in the DC/DC Full Bridge converter. These datasheets will aid in the connection of the components and integration into the DC/DC converter. Included in this section are the datasheets for the

- High Speed PWM Controller (UC3825BN)
- High and Low Side Driver (IR2110)
- Power MOSFET (IRFPS3810)
- Precision Lowest Cost Isolation Amplifier (ISO124)
- Current Transducer (HTR 50)
- 30A, 1200V Stealth Diode (ISL9R30120G2)
- 600V 30A Fuse (KTK-R)